Remarks

Claims 1-11 and 13-15 remain in the application. Claim 12 is hereby canceled without prejudice. Claims 1 and 13-15 are hereby amended. No new matter is being added.

Double Patenting

Claim 12 was rejected on the basis of nonstatutory double patenting. Claim 12 is hereby canceled without prejudice. As such, applicants respectfully submit that this rejection is now moot.

Claim Rejections -- 35 USC 101

Claim 12-15 were rejected under 35 USC 101. As stated by the Examiner, "In claim 15 the program product needs to be stored on the computer readable medium in order to be acceptable under 35 USC 101. Claims 12-14 are 'compiler' claims which are programs ...."

Claim 15 is hereby amended in accordance with the Examiner's comments. Amended claim 15 now recites "A computer-readable program product stored on a computer-readable medium ...." Hence, applicants respectfully submit that this rejection is now overcome with respect to claim 15.

Claim 12 is hereby canceled without prejudice. Claims 13 and 14 is hereby amended to incorporate the limitations of claim 12. Claims 13 and 14 are hereby amended in accordance with the Examiner's comments. Amended claims 13 and 14 now recite, "A program compiler stored on a computer-readable medium ...." Hence, applicants respectfully submit that this rejection is now overcome with respect to claims 13 and 14.

Claim Rejections--35 USC 103

Fruehling et al in view of Raina

Claims 1, 2, 5, 9-12, 14 and 15 were rejected under 35 U.S.C. 103 as being unpatentable over Fruehling et al (USP 6,625,688) in view of Raina (USP 6,134,675).

Discussion of claim 1

Amended claim 1 now recites as follows.

1. A method of **compiling** a program to be executed on a target microprocessor, the method comprising:

identifying, **while compiling the program**, a cycle during which a **functional unit** in the microprocessor would otherwise be idle;

opportunistically **scheduling, during compilation of the program,** a diagnostic operation for execution on the functional unit during said identified cycle; and

scheduling, during compilation of the program, a comparison of a result from executing the diagnostic operation with a corresponding predetermined result.

(Emphasis added.)

Applicants respectfully submit that Fruehling et al relates to a very different area of technology than the claimed invention. As seen above, the claimed invention relates to "[a] method of **compiling a program** to be executed on a target microprocessor ...." (Emphasis added.) In contrast, Fruehling et al discloses "a **circuit** for determining the health of a microcontroller" where the circuit "includes a bus, a CPU coupled to the bus and a register coupled to the bus." (Abstract of Fruehling et al, emphasis added.) Hence, applicant respectfully submits that Fruehling et al does not disclose or teach a technique relating to the same technological area as the claimed invention.

As discussed below, applicants respectfully submit that the various limitations of amended claim 1 are not taught by the cited combination of Fruehling et al in view of Raina.

1st Limitation

The first limitation of claim 1 recites "identifying, **while compiling the program**, a cycle during which a **functional unit** in the microprocessor would otherwise be idle." (Emphasis added.) In other words, **during program compilation**, a cycle is identified in which **a functional unit within a processor** would normally be idle.

In contrast, the cited portion of Fruehling in relation to the first limitation is column 12, lines 60-65. That citation recites the following.

> For the following example, it is presumed that **if the Parallel Signature Analysis (PSA) system is to work in background mode, the system must be able to either detect when the CPU has an idle cycle, force an idle cycle or stall the CPU.** Of course, the system may be configured to work in the foreground mode as well.
>
> (Emphasis added.)

The **PSA system** referred to above relates to the **circuitry which analyzes signatures generated in response to memory**. (See Abstract, Fruehling et al.) As recited above, in order to work in a background mode, "**the system must be able to either detect when the CPU has an idle cycle, force an idle cycle or stall the CPU**." In other words, Fruehling et al teaches **circuitry** that may detect when the **CPU** (not just a functional unit in the CPU) is actually idle.

Hence, the first claim limitation is substantially distinguished over the cited teaching of Fruehling et al. In particular, the first limitation pertains to identification by a **compiler** of a processor cycle in which a **functional unit** would otherwise be idle. In contrast, the cited teaching of Fruehling et al relates to **circuitry** that may detect when the **CPU** (not just a functional unit in the CPU) is actually idle.

2nd Limitation

The second limitation of claim 1 recites "opportunistically **scheduling, during compilation of the program,** a diagnostic operation for execution on the functional unit during said identified cycle." (Emphasis added.) In other words, **during program compilation**, the compiler **schedules** a diagnostic operation for execution during the cycle identified in the first limitation. Note that said identified cycle is a **cycle of operation of a functional unit within a processor**.

In contrast, the cited portion of Fruehling in relation to the second limitation is column 11, lines 32-34. That citation recites the following. "In state 4, the PSA Mode Controller may steal a bus cycle or **use idle bus cycles, if available**." (Emphasis added.) In other words, the citation relates to a **controller** stealing or using idle **bus cycles**. Note that **bus cycles** pertain to cycles on a communication bus **between a microprocessor and other devices** (i.e. outside a microprocessor).

Hence, the second claim limitation is substantially distinguished over the cited teaching of Fruehling et al. In particular, the second claim limitation pertains to the **scheduling** by a **program compiler** of a diagnostic operation on an otherwise idle **functional unit cycle**. In contrast, the cited teaching of Fruehling et al relates to a **controller stealing or using idle bus cycles**.

3rd Limitation

The third limitation of claim 1 recites "**scheduling, during compilation of the program,** a comparison of a result from executing the diagnostic operation with a corresponding predetermined result." (Emphasis added.) In other words, **during program compilation**, the compiler **schedules** a comparison operation after the diagnostic operation from the second limitation.

In contrast, Raina relates to a "method and device for **testing** multi-core processor integrated circuits." (Column 1, lines 22-23, emphasis added.) Raina teaches a **testing device 12** which receives **input signals 24, 26, 28,** and **30** from **multiple processor cores 14**. (FIG. 1 and Column 2, lines 7-9, emphasis added.)

Hence, the third claim limitation is substantially distinguished over the cited teaching of Raina. In particular, the third claim limitation pertains to the

scheduling of a comparison operation by a **compiler**. In contrast, the cited teaching of Raina relates to a **testing device** which receives **input signals** from **multiple processor cores**.

Conclusion for Claim 1

For at least the above-discussed reasons, applicants respectfully submit that claim 1 is now patentably distinguished over the cited art.

Claims 2, 5, and 9-11

Claims 2, 5, and 9-11 depend from claim 1. Hence, for at least the reasons discussed above in relation to claim 1, applicants respectfully submit that claims 2, 5, and 9-11 are also now patentably distinguished over the cited art.

Claims 14-15

Similar to claim 1, claim 14 pertains to a **program compiler** which includes a **scheduler**. The scheduler "identifies a cycle during which a **functional unit** would otherwise be idle, opportunistically **schedules** a diagnostic operation to be executed on the functional unit during that cycle, and **schedules** a comparison of a result from executing the diagnostic operation with a corresponding predetermined result." (Emphasis added.) Hence, applicants respectfully submit that claim 14 is now patentably distinguished over the cited art for similar reasons as discussed above in relation to claim 1.

Also similar to claim 1, claim 15 pertains to a "**program product** comprising executable code that includes a diagnostic operation **scheduled** for a **functional unit** that would otherwise be idle during a cycle and also includes a subsequently **scheduled** comparison of a result from executing the diagnostic operation with a corresponding predetermined result." (Emphasis added.) Hence, applicants respectfully submit that claim 15 is now patentably distinguished over the cited art for similar reasons as discussed above in relation to claim 1.

Fruehling et al in view of Raina further in view of Quach

Claims 3, 4, 6-8 and 13 were rejected under 35 U.S.C. 103 as being unpatentable over Fruehling et al (USP 6,625,688) in view of Raina (USP 6,134,675) and further in view of Quach (USP 6,640,313).

Discussion of Quach

Quach discloses a "Microprocessor with a High-Reliability Operating Mode." (Title of Quach.) Quach teaches a **microprocessor** that operates in high-reliability or high-performance modes in response to **mode switch events**. (See Abstract of Quach.)

Applicants respectfully submit that Quach does not disclose or teach the limitations of amended claim 1. In particular, Quach does not teach the first limitation of "identifying, **while compiling the program**, a cycle during which a **functional unit** of multiple functional units of a same type in the microprocessor would otherwise be idle." (Emphasis added.) Nor does Quach teach the second and third limitations of "opportunistically **scheduling, during compilation of the program,** a diagnostic operation for execution on the functional unit during said identified cycle" and "**scheduling, during compilation of the program,** a comparison of a result from executing the diagnostic operation with a corresponding predetermined result." (Emphasis added.)

Claims 3, 4, and 6-8

Claims 3, 4, and 6-8 depend from claim 1. Hence, for at least the reasons discussed above in relation to claim 1, applicants respectfully submit that claims 3, 4, and 6-8 are also now patentably distinguished over the teachings of Fruehling et al in view of Raina further in view of Quach.

Claim 13

Similar to claim 1, claim 13 pertains to a **program compiler** which includes a **scheduler**. The scheduler "identifies a cycle during which a functional unit would otherwise be idle, opportunistically **schedules** a diagnostic operation to be executed on the functional unit during that cycle, and **schedules** a comparison of a result from executing the diagnostic operation with a corresponding predetermined result." (Emphasis added.) Hence, for similar

reasons as discussed above in relation to claim 1, applicants respectfully submit that claim 13 is now patentably distinguished over the teachings of Fruehling et al in view of Raina further in view of Quach.

Conclusion

For the above-discussed reasons, applicant believes that claims 1-11 and 13-15, as they are hereby amended, are now patentably distinguished over the cited art. Favorable action is respectfully requested.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 08-2025.

Respectfully Submitted,

DALE JOHN SHIDLA et al.

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